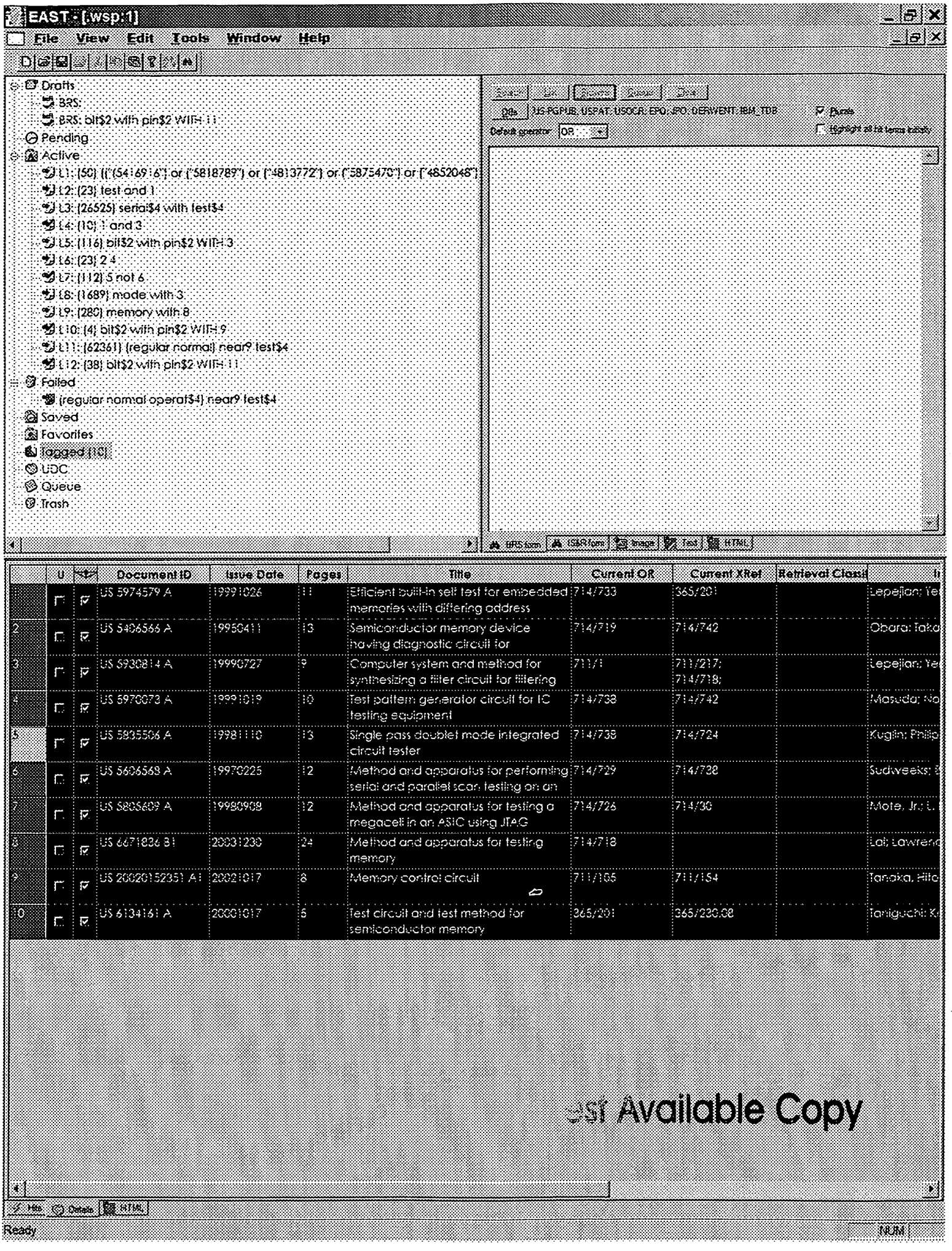

	U	T	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classi	
1			US 5974579 A	19991026	11	Efficient built-in self test for embedded memories with differing address	714/733	365/201		Lepejian; Ye
2			US 5406566 A	19950411	13	Semiconductor memory device having diagnostic circuit for	714/719	714/742		Obara; Taka
3			US 5930814 A	19990727	9	Computer system and method for synthesizing a filter circuit for filtering	711/1	711/217; 714/718;		Lepejian; Ye
4			US 5970073 A	19991019	10	Test pattern generator circuit for IC testing equipment	714/738	714/742		Masuda; No
5			US 5835506 A	19981110	13	Single pass doublet mode integrated circuit tester	714/738	714/724		Kuglin; Philip
6			US 5606569 A	19970225	12	Method and apparatus for performing serial and parallel scan testing on an	714/729	714/738		Sudweeks; S
7			US 5805609 A	19980908	12	Method and apparatus for testing a megacell in an ASIC using JTAG	714/726	714/30		Mote, Jr.; L
8			US 6671836 B1	20031230	24	Method and apparatus for testing memory	714/718			Lai; Lawren
9			US 20020152351 A1	20021017	8	Memory control circuit	711/105	711/154		Tanaka, Hito
10			US 6134161 A	20001017	6	Test circuit and test method for semiconductor memory	365/201	365/230.08		Taniguchi; K

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